OVERVIEW

This application note covers five topics concerning Dallas Semiconductor framers and single-chip transceivers (SCTs). The first section provides a detailed explanation about how the framer or SCT synchronize to an incoming data stream. This section also defines the resync criteria and how a resync is performed. The second section explains how the framer or SCT can be set up to sync to a data stream when it is not known beforehand whether CAS or CRC4 multiframes are present in the data stream. The third section shows how a user can determine what frame or multiframe level caused a loss-of-synchronization. The fourth section demonstrates how to decode the receive frame-error pin on a framer or SCT. Finally, the fifth section is a short tutorial on E1 frame and multiframe structures.

SECTION 1: HOW FRAMERS AND SCTs SYNC AND RESYNC

In an E1 mode, the data stream always contains the frame alignment signal (FAS), and it can contain either one or both of the two kinds of multiframe, namely cyclic redundancy check 4 (CRC4) and channel associated signaling (CAS). The following discussion covers how Dallas framers and SCTs handle synchronization and resynchronization under FAS, CRC4, and CAS levels. Refer to Figures 1A and 1B as a supplement to the discussion.

FAS Sync

The framer or SCT always begins a sync or resync with a search for the FAS. The framer or SCT considers that it has found the FAS when it has located a correct FAS word (X0011011), followed by a non-FAS word with bit 2 set to a 1 (X1XXXXXX), followed by another correct FAS word. If a proper FAS sequence exists in the incoming data stream, then the framer or SCT syncs to it in, at most, four frames or 500ms. If a resync is occurring (i.e., the part has previously obtained FAS sync), the framer or SCT begins a bit-by-bit search for the FAS word in the time slot following the one to which it had previously been aligned. This reduces the chance of the framer resyncing onto the same emulator. If both CAS and CRC4 are disabled, once the FAS sync criteria is met, the framer or SCT enters a sync condition and the receive loss-of-sync (RLOS) pin goes low. If either CAS or CRC4 is enabled, then the framer or SCT performs a search for its respective multiframe alignment signals before a sync condition is asserted. If both CAS and CRC4 are enabled, then the searches are performed in parallel after the FAS sync criteria has been met.

CAS Multiframe Sync

If CAS is enabled, then the framer or SCT uses the frame alignment created by the FAS sync to locate time slot 16. The framer then begins searching time slot 16 for the multiframe alignment word (0000XXXX). If the framer or SCT finds the frame alignment word and the previous time slot 16 did not contain the multiframe alignment word, then CAS multiframe sync is declared. The user has the option of making the CAS sync criteria more rigid by setting the CAS multiframe sync criteria bit. If the multiframe sync criteria bit is set, then the framer or SCT looks for two additional multiframe alignment words before it declares sync. In the SYNC/RSYNC flow without the CAS multiframe-sync criteria bit set to low, if the framer or SCT cannot find CAS multiframe alignment in 12ms to 14ms (i.e., over six

full multiframes), then it sets the frame resync criteria enabled and initiates a resync at the FAS level. In the SYNC/RSYNC flow when the CAS multiframe sync-criteria bit set to hight, the device continuously searches for the CAS multiframe alignment.

CRC4 Multiframe Sync

If CRC4 is enabled, then the framer or SCT searches for the CRC4 multiframe alignment word (001011XX) in bit 1 of time slot 0 of the nonalign frames. In the SYNC/RSYNC flow, in one sync algorithm, if two valid multiframe alignment words are found in 12ms to 14ms, then sync is declared. Otherwise, in another sync algorithm, the framer or SCT initiates a resync at the FAS level. In the SYNC/RSYNC flow with E1 mode, the time out period is reduced to 8ms.

FAS Resync Criteria

Once sync is declared, then the framer or SCT, in E1 mode, automatically monitors the FAS words for errors. If the FAS word is received in error three consecutive times, then the frame resync criteria is met. It shows in the status register, and a resync is initiated if the sync enable bit is cleared. The user can make the resync criteria softer by enabling the frame resync criteria bit. If the frame resync criteria bit is enabled, then the framer or SCT monitors bit 2 in time slot 0 of the nonalign frames as well as the FAS words for errors. If either bit 2 or the FAS word (or both) is incorrect on three consecutive occasions, then a resync is initiated.

CAS Resync Criteria

If CAS is enabled, then the framer or SCT monitors time slot 16 for errors in the multiframe alignment word. If two consecutive multiframe alignment words are received in error, the CAS multiframe resync-criteria bit is then set to a 1. But, if the sync bit is enabled, then a resync at the FAS level is initiated. The CAS resync criteria can be softened by setting CAS multiframe criteria bit to 1. When this bit is set, then the framer or SCT resyncs if it gets two incorrect multiframe alignment words in a row or if it ever receives two consecutive time slot 16 words with 0s in the first four MSB bit positions (0000XXXX).

CRC4 Resync Criteria

Once the framer or SCT has achieved sync, if CRC4 is enabled, it then begins recording CRC4 code word errors in the CRC4 count error register (CECR). CCITT recommends that if more than 914 CRC4 errors are received out of a block of 1000 code words, that it is to be assumed that the framer has falsely locked onto an emulator and a resynchronization should be initiated. In one of the sync algorithm modes, there is an automatic CRC4 resync criteria that forces a resynchronization if 915 or more CRC4 code words, out of a 1000, are received in error. But, in another sync algorithm more, the user can monitor CRC4 code-word errors in the CECR or the RFER pins and initiate a resync in the framer or SCT by toggling resync bit from a 0 to a 1 or by doing a hardware reset.

Figure 1A. Framers and SCTs sync/resync flow without CRC4 sync time out to 12ms and with a time-out period for CAS multiframe search.
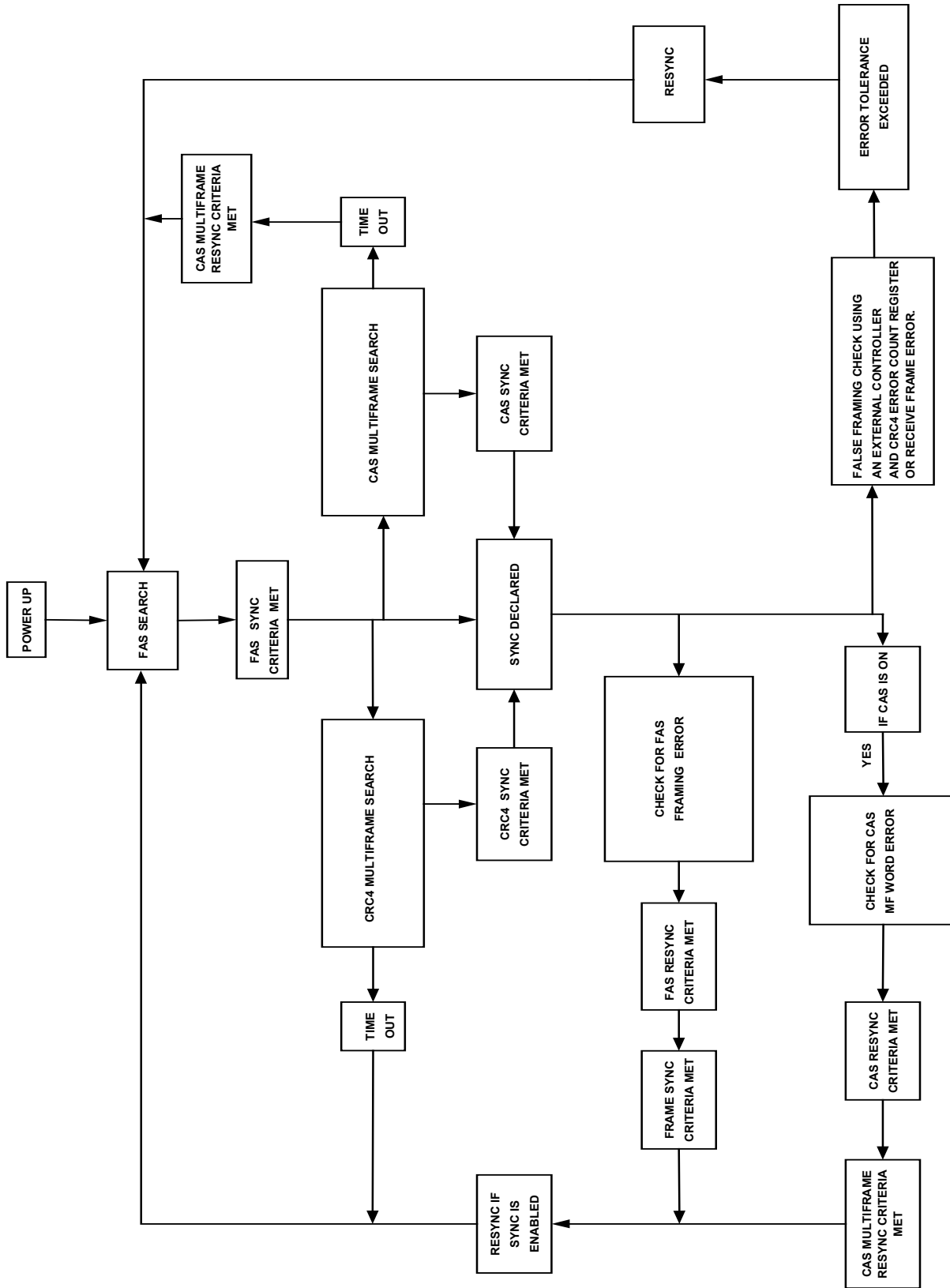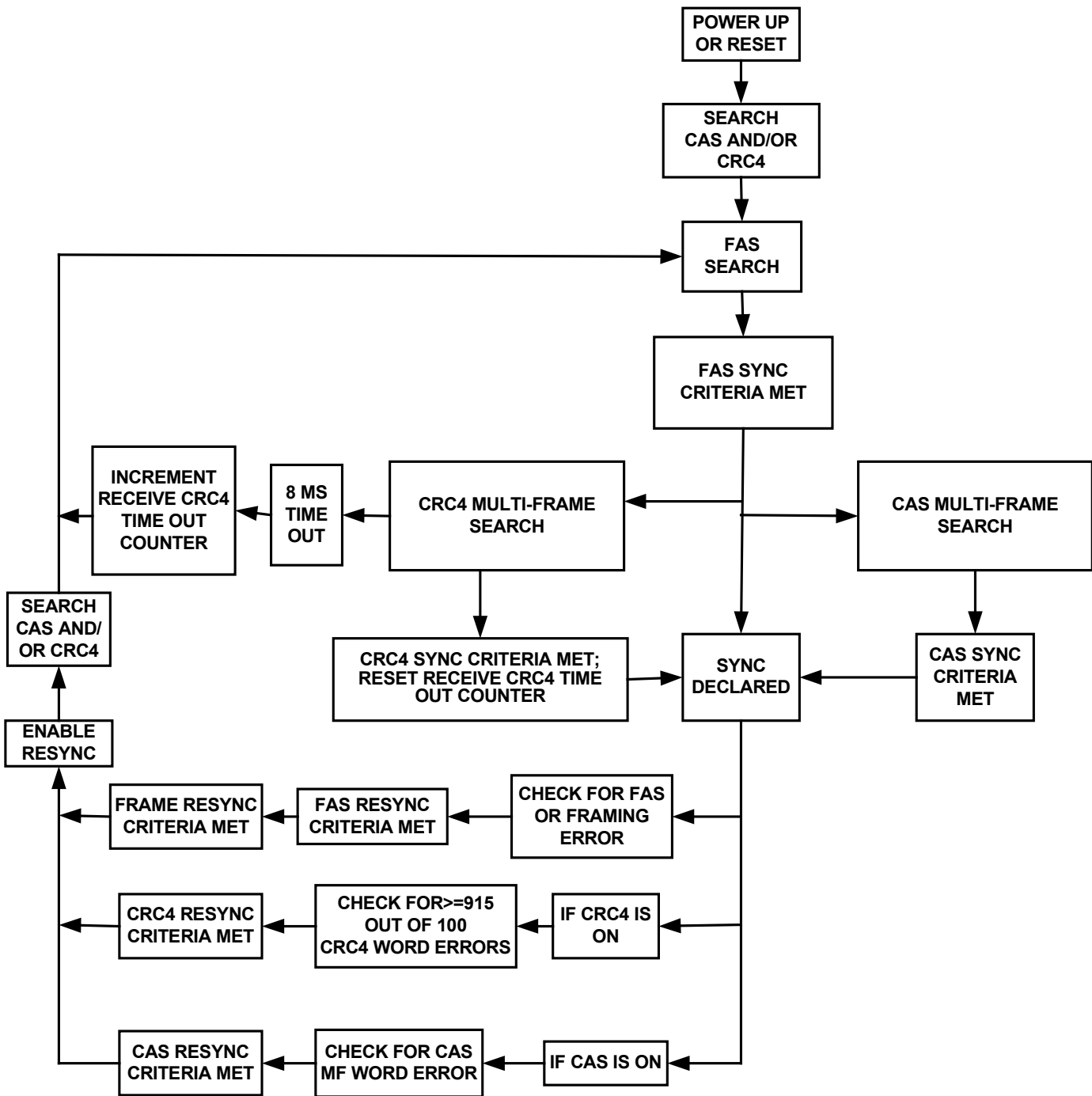
Figure 1B. Framers and SCTs sync/resync flow with CRC4 sync time out to 8ms and without a time-out period for CAS multiframe search.

```
                                              POWER UP
                                              OR RESET
                                                  │
                                                  ▼
                                               SEARCH
                                            CAS AND/OR
                                               CRC4
                                                  │
                                                  ▼
                                                FAS
                                               SEARCH
                                                  │
                                                  ▼
                                             FAS SYNC
                                          CRITERIA MET

INCREMENT      8 MS     CRC4 MULTI-FRAME                  CAS MULTI-FRAME
RECEIVE CRC4   TIME     SEARCH                            SEARCH
TIME OUT       OUT
COUNTER

SEARCH       CRC4 SYNC CRITERIA MET;        SYNC          CAS SYNC
CAS AND/     RESET RECEIVE CRC4 TIME       DECLARED       CRITERIA
OR CRC4      OUT COUNTER                                  MET

ENABLE
RESYNC

FRAME RESYNC    FAS RESYNC     CHECK FOR FAS
CRITERIA MET    CRITERIA MET   OR FRAMING
                               ERROR

CRC4 RESYNC    CHECK FOR>=915   IF CRC4 IS
CRITERIA MET   OUT OF 100       ON
               CRC4 WORD ERRORS

CAS RESYNC     CHECK FOR CAS    IF CAS IS ON
CRITERIA MET   MF WORD ERROR
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SECTION 2: Using Framers and SCTs to Determine Sync Frame/Multiframe Conditions

The framer or SCT can be used to determine whether or not the incoming data stream contains any of the following:

- channel associated signaling (CAS) multiframe structure
- cyclical redundancy check 4 (CRC4) multiframe structure
- frame alignment signal (FAS) frame structure

In order to establish which of the three are present, the user must selectively enable and disable the various multiframe modes of the framer or SCT. One possible method of performing this function is shown in a flow chart in Figure 2. The flow chart suggests that the user initially enable both CAS and CRC4 multiframes and try to achieve sync. If sync cannot be obtained, then first CAS is disabled and then CRC4 is disabled. If sync still cannot be obtained, then the FAS structure must not be present. Users can implement the flow chart outlined in Figure 2 with the framer or SCT in either hardware or software mode.

In Dallas Semiconductor devices like DS2154, DS21X54, DS2155, DS21Q44, and DS2156, the host only needs to read the SYNC status registers (INFO3 and INFO7) to determine these above conditions.

CAS Resync Criteria Met Event (CASRC). Set when two consecutive CAS MF alignment words are received in error.

FAS Resync Criteria Met Event (FASRC). Set when three consecutive FAS words are received in error.

CRC Resync Criteria Met Event (CRCRC). Set when 915/1000 code words are received in error.

CRC4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC4 MF alignment word.

CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

SECTION 3: Determining What Caused Resync

If the framer or SCT is used in software mode, then the receive status register can be monitored to determine what event triggered a loss of synchronization. One possible method of performing this task is shown in the form of a flowchart in Figure 3. The flow chart suggests that the user monitor the receive loss-of-sync bit (RLOS) or pin to ascertain when a loss of synchronization occurs. Once a loss of synchronization has occurred, then the use of the frame resync criteria bit and the CAS multiframe resync criteria bit along with the known configuration of the transceiver can be used to establish the event that evoked the loss of synchronization.

SECTION 4: Decoding the Receive Frame-Error Pin on Framers and SCTs

Three types of errors in the received data stream are reported in real time at the receive frame-error pin.

1) Errors in the frame alignment signal (FAS) word
2) Errors in the channel associated signaling (CAS) multiframe alignment word
3) Errors in the cyclical redundancy check 4 (CRC4) code word

The user can determine the type of error reported at the receive frame-error pin by externally decoding the pin with two AND gates and a D-type flip flop, as shown in Figure 4. A rising edge out of either the AND gates or the D-type flip flop indicates that a particular error event has occurred.

SECTION 5: E1 Frame and Multiframe Structures

E1 Frame Structure

The 2.048MHz E1 (PCM–30) environment consists of a frame structure of 256 bits that is repeated at an 8kHz rate. Each frame consists of 32 8-bit time slots that are numbered from 0 to 31. The first eight bits of every frame (time slot 0) are used mainly to provide framing information. Every other time slot 0 contains a fixed 7-bit pattern known as the frame alignment signal (FAS) (Figure 5). As its name suggests, the FAS pattern (X0011011) identifies time slot 0, from which the other time slots can be readily ascertained. In frames that do not begin with the FAS (nonalign frames), bit 2 of the time slot is fixed at a 1 to ensure that it does not emulate the FAS pattern. Besides framing information, time slot 0 contains two sets of spare bits and an alarm. One spare bit per frame is intended for international use and it is designated Si in Figure 5. Five spare bits per frame are available for national usage and they are designated Sa in Figure 5. Bit 3 of the nonalign frames is used to indicate whether the remote unit is in alarm or not. If the alarm bit is set to a 1, then an alarm condition exists at the remote. If it is 0, then no alarm condition exists.

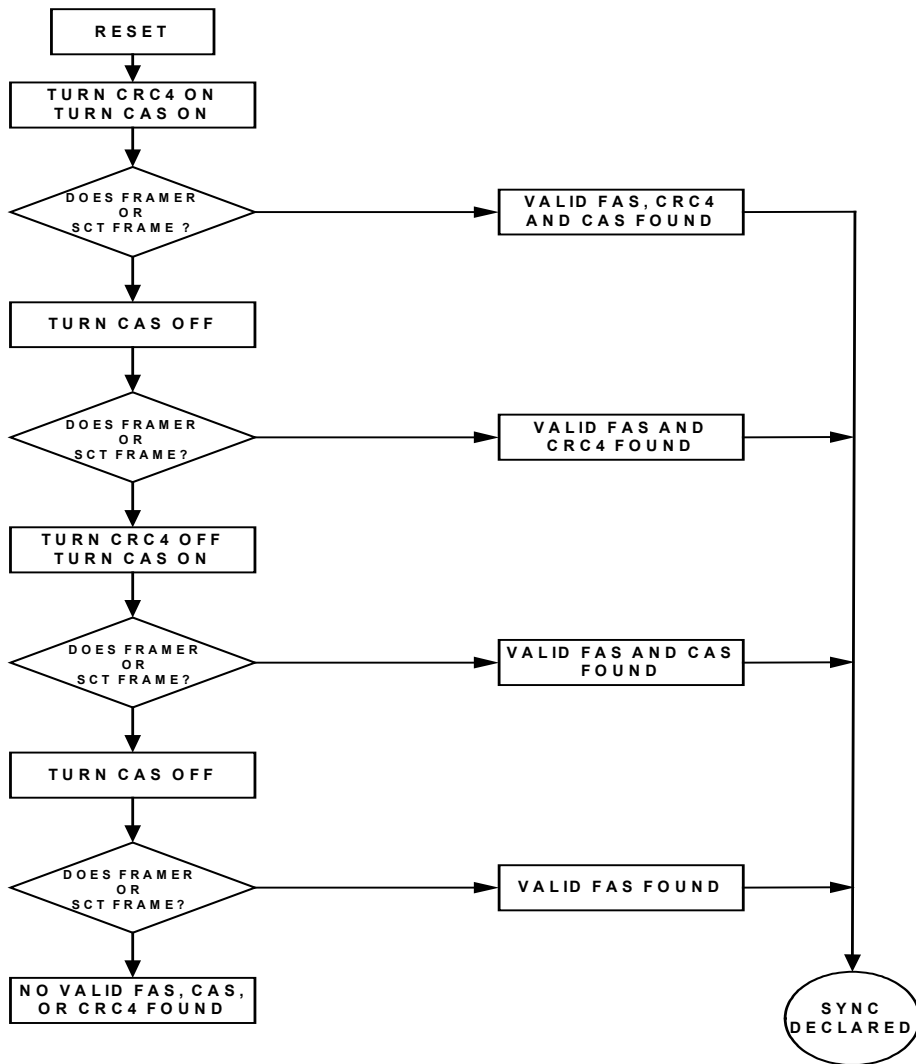**Figure 2: Flowchart to Determine Frame/Multiframe**

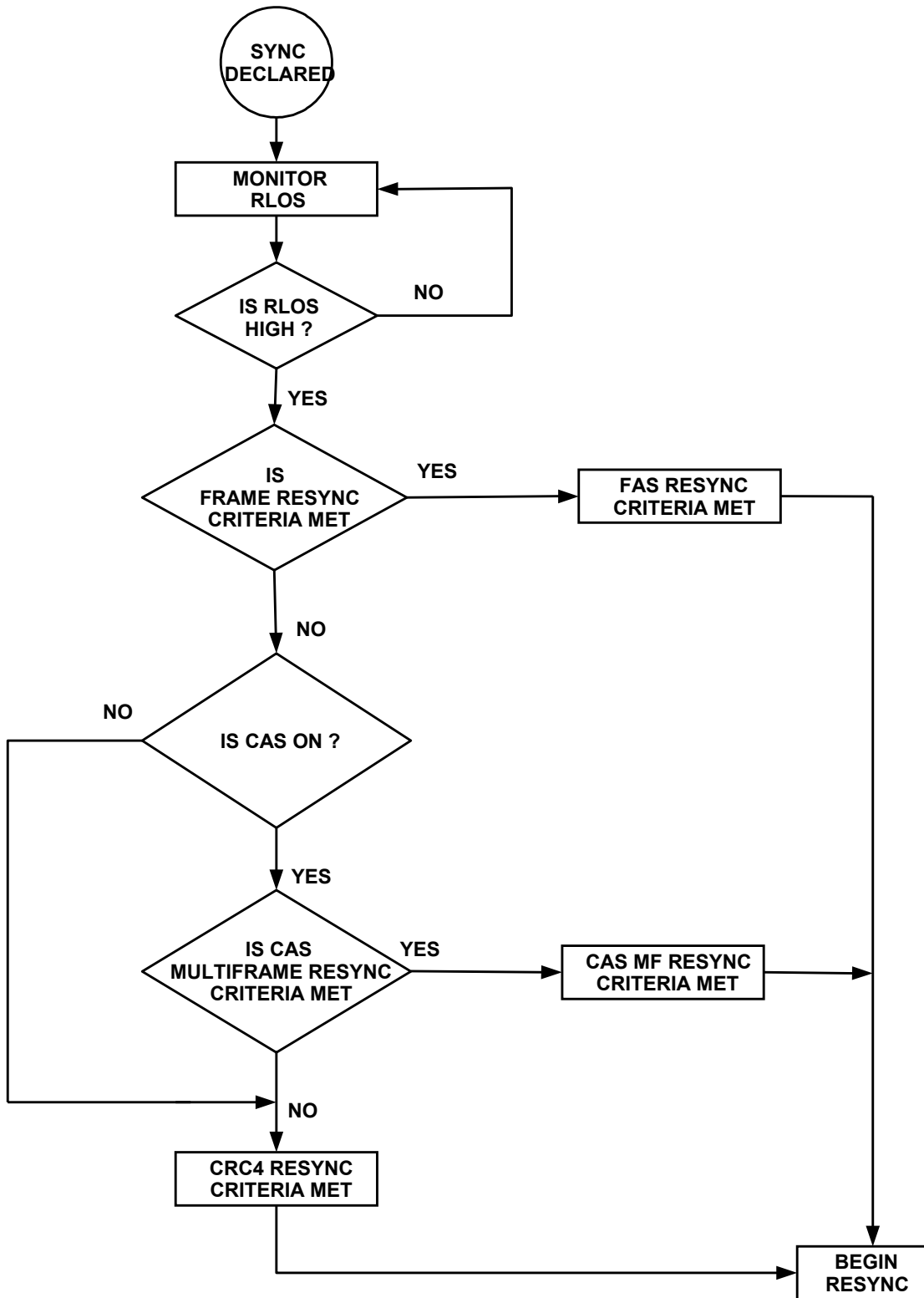**Figure 3. Framers and SCTs Flowchart for Loss-of-Sync**

Figure 4. Externally Decoding the Receive Frame-Error Pin

Figure 5. E1 Frame Structure

1 FRAME = 32 TIME SLOTS = 256 BITS

TIME SLOT 0

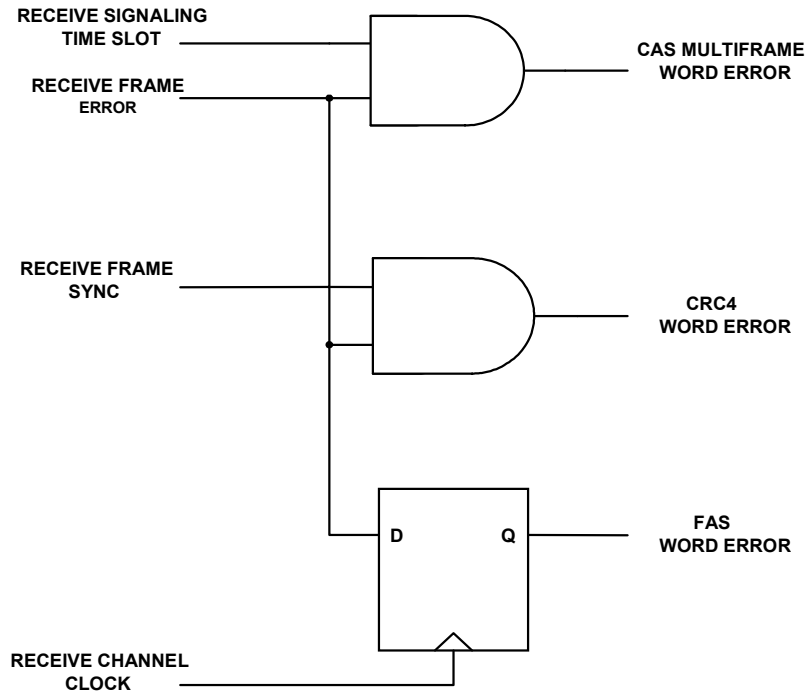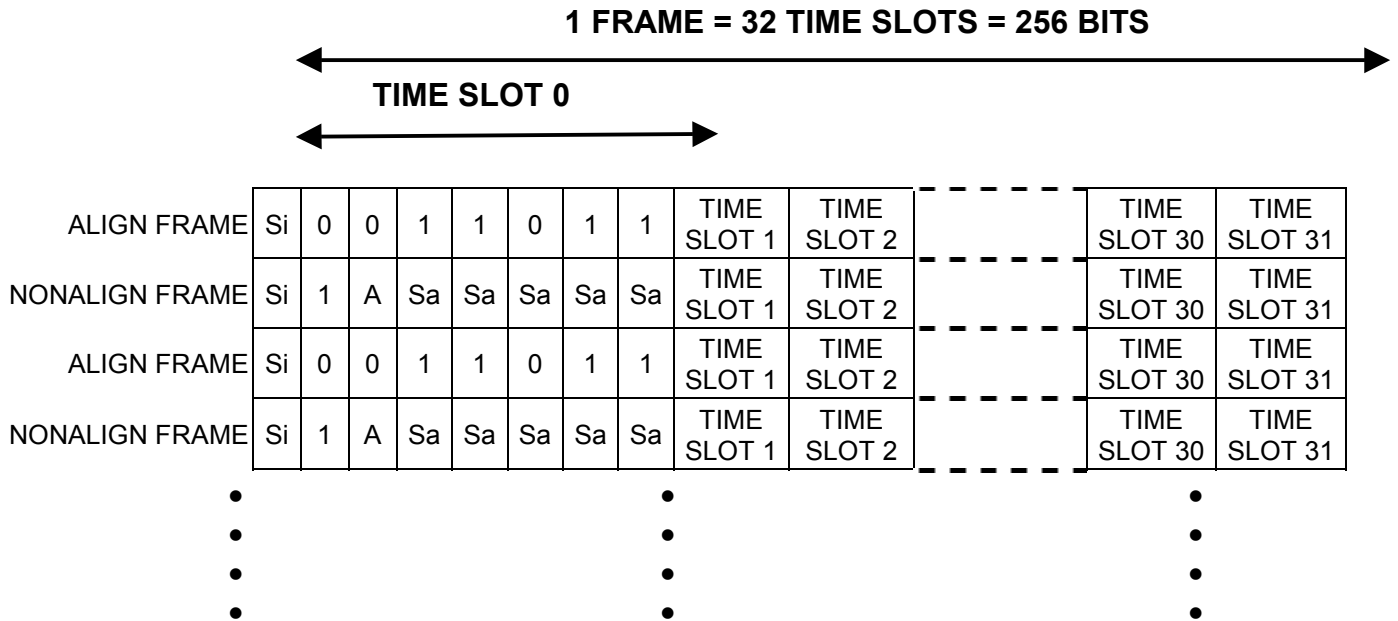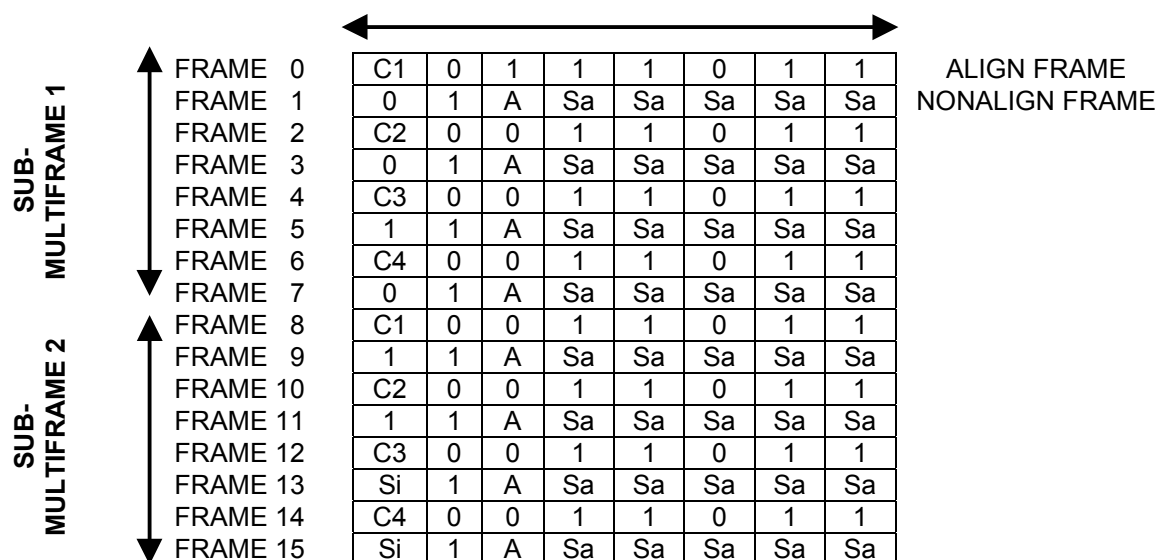|												
ALIGN FRAME	Si	0	0	1	1	0	1	1	TIME SLOT 1	TIME SLOT 2	TIME SLOT 30	TIME SLOT 31
NONALIGN FRAME	Si	1	A	Sa	Sa	Sa	Sa	Sa	TIME SLOT 1	TIME SLOT 2	TIME SLOT 30	TIME SLOT 31
ALIGN FRAME	Si	0	0	1	1	0	1	1	TIME SLOT 1	TIME SLOT 2	TIME SLOT 30	TIME SLOT 31
NONALIGN FRAME	Si	1	A	Sa	Sa	Sa	Sa	Sa	TIME SLOT 1	TIME SLOT 2	TIME SLOT 30	TIME SLOT 31

E1 Multiframe Structure

Two separate multiframe structures exist in E1 environments, cyclical redundancy check 4 (CRC4) and channel associated signaling (CAS). Both of these multiframes are based on the FAS framing level, but they are used independently of each other for different purposes. Although both multiframes consist of a set of 16 consecutive frames, they need not be aligned nor must they both be present in a data stream.

CRC4 Multiframe Structure

The multiframe structure of CRC4 is shown in Figure 6. The CRC4 multiframe consists of a multiframe alignment word and two 4-bit code words. The CRC4 multiframe always begins on an align frame and it uses the spare international bit (bit 1 of both align and nonalign frames) location. The CRC4 multiframe alignment word is a repeating 6-bit code (001011) that is located in odd frames 1 through 11. Each CRC4 multiframe is divided into two submultiframes (SMF). Each SMF consists of eight frames and contains one 4-bit CRC4 code word. Each code word represents a data check on eight frames on data (8 frames X 256 bits/frame = 2048 bits). Each eight-frame set is called a block. Hence, each SMF is equivalent to one block. The two 4-bit code words are located in the even frames. The CRC4 multiframe is used primarily to assist in validating alignment at the FAS level but it could also be used to monitor error performance. CCITT recommends that whenever more than 914 CRC4 blocks out of 1000 are received in error, then it should be assumed that a false alignment at the FAS level has occurred.

Figure 6. CRC4 Multiframe Structure

SUB-MULTIFRAME 1	FRAME 0	C1	0	1	1	1	0	1	1	ALIGN FRAME
	FRAME 1	0	1	A	Sa	Sa	Sa	Sa	Sa	NONALIGN FRAME
	FRAME 2	C2	0	0	1	1	0	1	1
	FRAME 3	0	1	A	Sa	Sa	Sa	Sa	Sa
	FRAME 4	C3	0	0	1	1	0	1	1
	FRAME 5	1	1	A	Sa	Sa	Sa	Sa	Sa
	FRAME 6	C4	0	0	1	1	0	1	1
	FRAME 7	0	1	A	Sa	Sa	Sa	Sa	Sa
SUB-MULTIFRAME 2	FRAME 8	C1	0	0	1	1	0	1	1
	FRAME 9	1	1	A	Sa	Sa	Sa	Sa	Sa
	FRAME 10	C2	0	0	1	1	0	1	1
	FRAME 11	1	1	A	Sa	Sa	Sa	Sa	Sa
	FRAME 12	C3	0	0	1	1	0	1	1
	FRAME 13	Si	1	A	Sa	Sa	Sa	Sa	Sa
	FRAME 14	C4	0	0	1	1	0	1	1
	FRAME 15	Si	1	A	Sa	Sa	Sa	Sa	Sa

CAS Multiframe Structure

Figure 7 shows the CAS multiframe structure. It is made up of 16 frames and can begin on either an align or a nonalign frame. The CAS multiframe always resides in time slot 16. The first frame contains a multiframe alignment word (0000) in the upper nibble and a set of spare and alarm bits (xyxx) in the lower nibble. The spare bits are denoted as "x" and should be set to a 1 if they are not being used. The alarm bit is denoted as "y" and is set to a 1 if CAS multiframe alignment is lost. The other 15 frames contain 30 channels of signaling data as demonstrated in Figure 7. If the B, C, and D bits are not used, then they should be set to 1, 0, and 1, respectively.

Figure 7. Multiframe Structure